National Semiconductor

Bipolar PROMs

DM54S570/DM74S570 2048-Bit (512 x 4) Open-Collector PROM

DM54S571/DM74S571 2048-Bit (512 x 4) TRI-STATE® PROM

General Description

These Schottky memories are organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

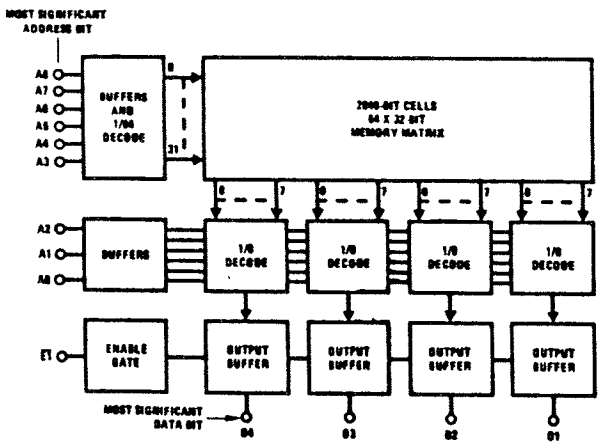
See the last page of this section for detailed programming information.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—55 ns max
  Enable access—30 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM74S270 and DM74S370

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S570		X	X		N, J
DM74S571		X		X	N, J
DM54S570	X		X		J
DM54S571	X			X	J

Block Diagram

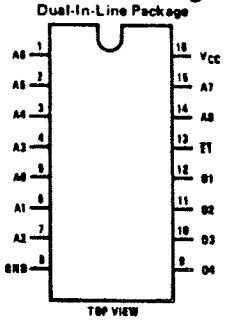


Order Number DM54S570J, DM54S571J, DM74S570J or DM74S571J
See NS Package J16A

Order Number DM74S570N or DM74S571N
See NS Package N16A

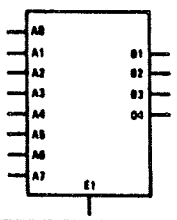
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



PAPETERIE DES ARTS + MÉTIERS - GENÈVE

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	-0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S570, DM54S571	4.5	5.5	V
DM74S570, DM74S571	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S570, DM54S571	−55	+125	°C
DM74S570, DM74S571	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S570, 54S571			DM74S570, 74S571			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		90	130		90	130	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S570, 54S571 5V ±10%; −55°C to +125°C			DM74S570, 74S571 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time	*(Figure 1)*		40	65		40	55	ns
t_{EA}	Enable Access Time	*(Figure 2)*		20	35		20	30	ns
t_{ER}	Enable Recovery Time	*(Figure 2)*		20	35		20	30	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

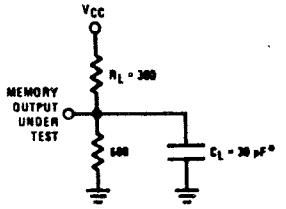
Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A8 and A2 (pin 14 and pin 7).

PAPETERIE DES ARTS + MÉTIERS - GENÈVE

Standard Test Load



*C_L includes probe and jig capacitance.

- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω, $t_r \leq 2.5$ ns and $t_f \leq 2.5$ ns (between 1.0V and 2.0V).
- t_{AA} is measured with both enable inputs at a steady low level.
- t_{EA} and t_{ER} are measured from the 1.5V on inputs and outputs with all address inputs at a steady level and with the unused enable input at a steady low level.

Switching Time Waveforms

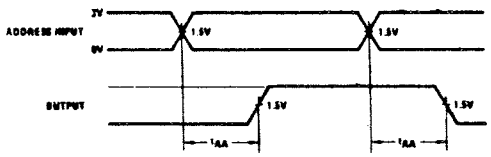


FIGURE 1. Address Access Time

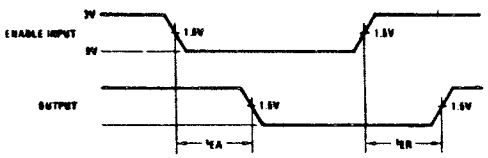
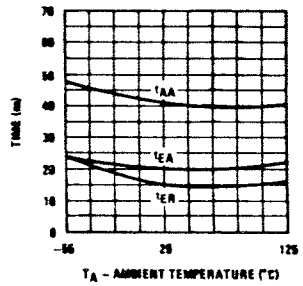


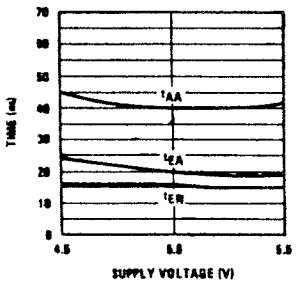
FIGURE 2. Enable Access Time and Recovery Time

Typical Performance Characteristics

Typical Switching Characteristics as a Function of Temperature (V_{CC} = 5V, Standard Load)

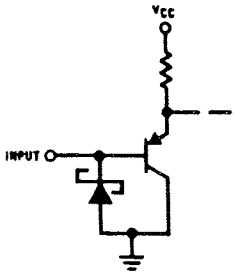


Typical Switching Characteristics as a Function of V_{CC} (T_A = 25°C, Standard Load)

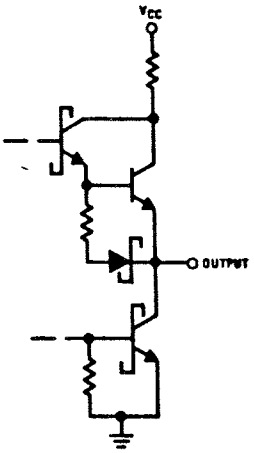


Equivalent Circuits

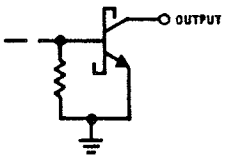
Equivalent of Each Input



Typical TRI-STATE Output



Typical Open-Collector Output



PAPETERIE DES ARTS + MÉTIERS - GENÈVE

National Semiconductor

Bipolar PROMs

DM54S572/DM74S572 4096-Bit (1024 x 4) Open-Collector PROM
DM54S573/DM74S573 4096-Bit (1024 x 4) TRI-STATE® PROM

General Description

These Schottky PROM memories are organized in the popular 1024 words by 4 bits configuration. Two memory enable inputs are provided to control the output states. When the enable inputs are in the low state, the outputs present the contents of the selected word.

If either or both of the enable inputs is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

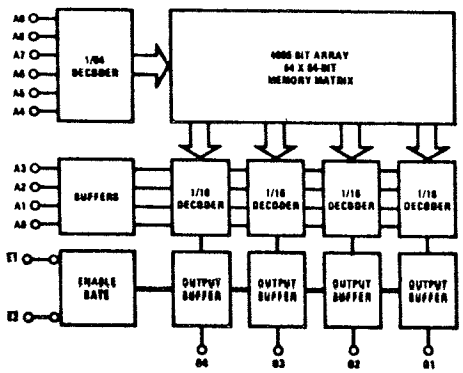
See the last page of this section for detailed programming information.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—60 ns max
  Enable access—35 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- High density 18-pin package

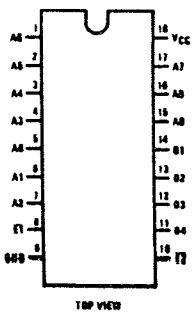
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S572		X	X		N,J
DM74S573		X		X	N,J
DM54S572	X		X		J
DM54S573	X			X	J

Block Diagram



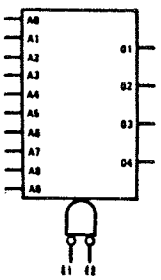
Connection Diagram

Dual-In-Line Package



Order Number DM54S572J, DM54S573J, DM74S572J or DM74S573J
See NS Package J18A

Logic Symbol



Order Number DM74S572N or DM74S573N
See NS Package N18A

PAPETERIE DES ARTS + MÉTIERS - GENÈVE

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S572, DM54S573	4.5	5.5	V
DM74S572, DM74S573	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S572, DM54S573	−55	+125	°C
DM74S572, DM74S573	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S572, 54S573			DM74S572, 74S573			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	µA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	µA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	µA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	µA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		125	140		125	140	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	µA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S572, 54S573 5V ±10%; −55°C to +125°C			DM74S572, 74S573 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			40	75		40	60	ns
t_{EA}	Enable Access Time			25	45		25	35	ns
t_{ER}	Enable Recovery Time			25	45		25	35	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A5 and A2 (pin 2 and pin 7).

PAPETERIE DES ARTS + MÉTIERS - GENÈVE

National Semiconductor

Bipolar PROMs

DM77S180/DM87S180, DM77S181/DM87S181
1024 x 8-Bit TTL PROM

General Description

These Schottky memories are organized in the popular 1024 words by 8 bits configuration. Four memory enable inputs are provided to control the output states. When $\overline{E1}$ and $\overline{E2}$ are low and E3 and E4 are high, the output presents the contents of the selected word.

If $\overline{E1}$ or $\overline{E2}$ are high, or E3 or E4 are low, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

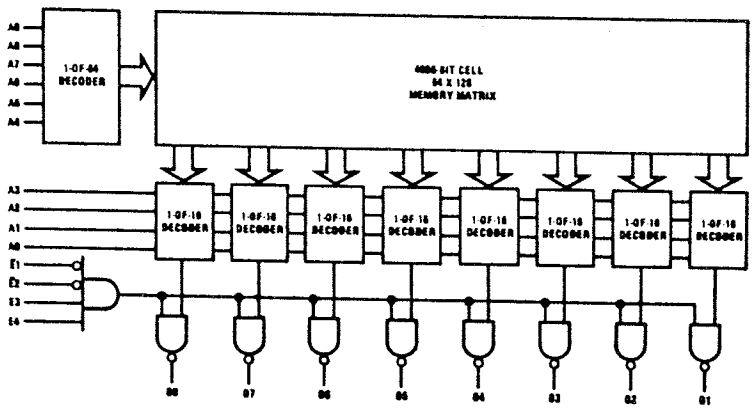
See the last page of this section for detailed programming information.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—40 ns typ
  - Enable access—15 ns typ
- PNP inputs reduce input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

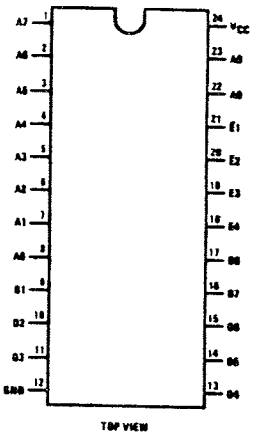
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87S180		X	X		N, J
DM87S181		X		X	N, J
DM77S180	X		X		J
DM77S181	X			X	J

Block Diagram

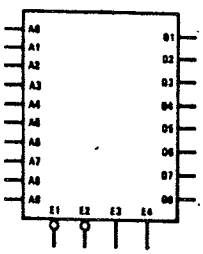


Connection Diagram

Dual-In-Line Package



Logic Symbol



Pin Names	
$\overline{E1}$ to E4	Enable Inputs
A0 to A9	Address Inputs
O1 to O8	Data Outputs

Order Number DM77S180J, DM77S181J, DM87S180J or DM87S181J
See NS Package J24A

Order Number DM87S180N or DM87S181N
See NS Package N24B

PAPETERIE DES ARTS + MÉTIERS - GENÈVE

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM77S180, DM77S181	4.5	5.5	V
DM87S180, DM87S181	4.75	5.25	V
Ambient Temperature (T_A)			
DM77S180, DM77S181	−55	+125	°C
DM87S180, DM87S181	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Parameter		Conditions	DM77S180, DM77S181			DM87S180, DM87S181			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−10	−100		−10	−100	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			50			50	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		115	170		115	170	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With standard load)

Parameter		Conditions	DM77S180, DM77S181 5V ± 10%; −55°C to +125°C			DM87S180, DM87S181 5V ± 5%, 0°C to +70°C			Units
			Min	Typ	Max	Min	Typ	Max	
t_{AA}	Address Access Time			40	75		40	60	ns
t_{EA}	Enable Access Time			15	35		15	30	ns
t_{ER}	Enable Recovery Time			15	35		15	30	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unles stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

PAPETERIE DES ARTS + MÉTIERS - GENÈVE

National Semiconductor

Bipolar PROMs

DM77S184/DM87S184 8192-Bit (2048 x 4) Open-Collector PROM
DM77S185/DM87S185 8192-Bit (2048 x 4) TRI-STATE® PROM

General Description

These Schottky PROM memories are organized in the popular 2048 words by 4 bits configuration. One memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

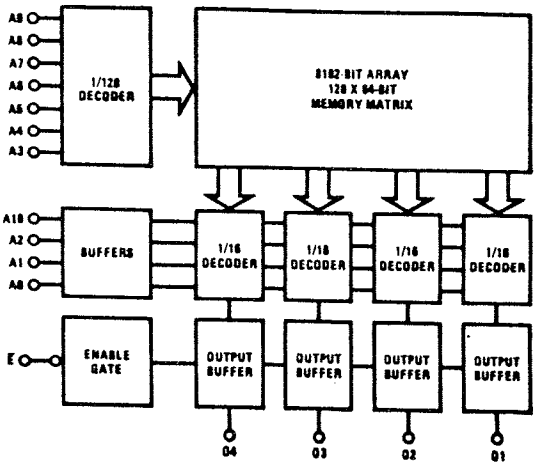
See the last page of this section for detailed programming information.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—40 ns max
  - Enable access—15 ns max
- PNP inputs reduce input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87S184		X	X		N, J
DM87S185		X		X	N, J
DM77S184	X		X		J
DM77S185	X			X	J

Block Diagram

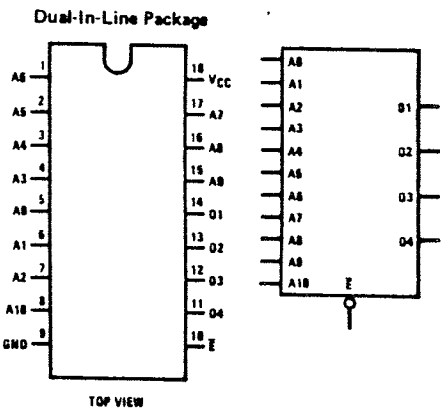


Pin Names

$\overline{E}$ Enable Input
A0-A10 Address Inputs
O1-O4 Data Outputs

Connection Diagram Logic Symbol

Dual-In-Line Package



Order Number DM77S184J, DM77S185J, DM87S184J or DM87S185J
See NS Package J18A

Order Number DM87S184N or DM87S185N
See NS Package N18A

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Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +6.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM77S184, DM77S185	4.5	5.5	V
DM87S184, DM87S185	4.75	5.25	V
Ambient Temperature (T_A)			
DM77S184, DM77S185	−55	+125	°C
DM87S184, DM87S185	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 3)

PARAMETER		CONDITIONS	DM77S184, DM77S185			DM87S184, DM87S185			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−10	−100		−10	−100	µA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	µA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			50			50	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	µA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	µA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		100	140		100	170	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	µA
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With standard load)

PARAMETER		CONDITIONS	DM77S184, DM77S185 5V ±10%, −55°C to +125°C			DM87S184, DM87S185 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			40	75		40	55	ns
t_{EA}	Enable Access Time			15	35		15	30	ns
t_{ER}	Enable Recovery Time			15	35		15	30	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

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National Semiconductor

Bipolar PROMs

DM77S188/DM87S188, DM77S288/DM87S288 32 × 8-Bit TTL PROM

General Description

These Schottky PROM memories are organized in the popular 32 words by 8 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

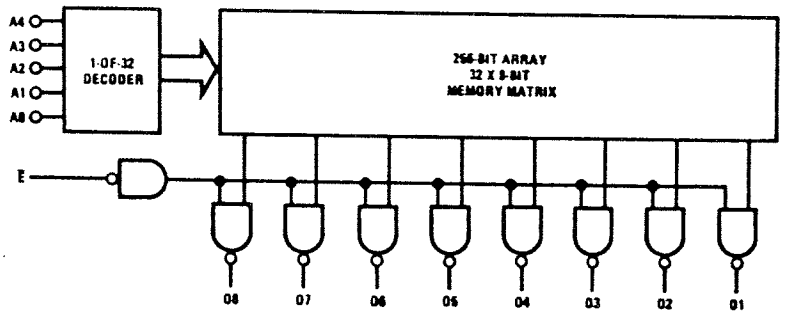
See the last page of this section for detailed programming information.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—12 ns typ
  - Enable access—8 ns typ
- PNP inputs reduce input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

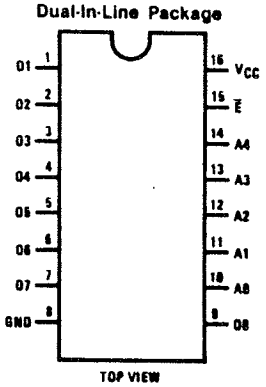
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87S188		X	X		N, J
DM87S288		X		X	N, J
DM77S188	X		X		J
DM77S288	X			X	J

Block Diagram



Connection Diagram

Dual-In-Line Package



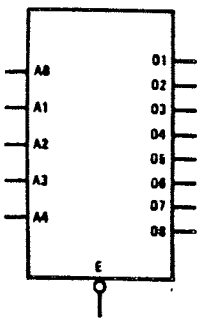
TOP VIEW

Order Number DM77S188J, DM77S288J, DM87S188J or DM87S288J
See NS Package J16A

Order Number DM87S188N or DM87S288N
See NS Package N16A

Pin Names	
$\overline{E}$	Enable Input
A0 to A4	Address Inputs
O1 to O8	Data Outputs

Logic Symbol



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